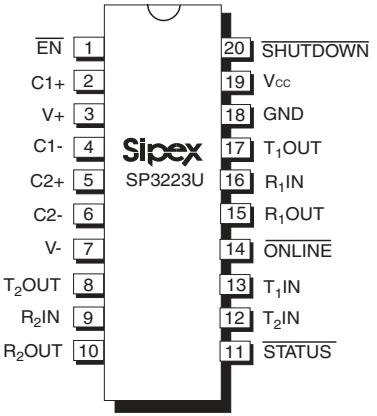
查询SP3223UCA供应商

High Speed Intelligent +3.0V to +5.5V RS-232 Transceivers

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Interoperable with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
- ***AUTO ON-LINE®*** circuitry automatically wakes up from a 1µA shutdown
- Regulated Charge Pump Yields Stable RS-232 Outputs Regardless of V_{CC} Variations
- ESD Specifications: ±2kV Human Body Model
- 1000 Kbps minimum transmission rate
- Ideal for High Speed RS-232 Applications



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DESCRIPTION

The SP3223U and SP3243U products are RS-232 transceiver solutions intended for portable or hand-held applications such as notebook and palmtop computers. The "U" series is based on Sipex's SP3223/SP3243 series and has been enhanced for high speed. The data rate is improved to 1000kbps, easily meeting the demands of high speed RS-232 applications. The SP3223U and SP3243U use an internal high-efficiency, charge-pump power supply that requires only 0.1µF capacitors in 3.3V operation. This charge pump and Sipex's driver architecture allow the SP3223U/SP3243U series to deliver compliant RS-232 performance from a single power supply ranging from +3.0V to +5.5V. The SP3223U is a 2-driver/2-receiver device, and the SP3243U is a 3-driver/5-receiver device, ideal for laptop/notebook computer and PDA applications. The SP3243U includes one complementary receiver that remains alert to monitor an external device's Ring Indicate signal while the device is shutdown.

The AUTO ON-LINE® feature allows the device to automatically "wake-up" during a shutdown state when an RS-232 cable is connected and a connected peripheral is turned on. Otherwise, the device automatically shuts itself down drawing less than 1µA.

SELECTION TABLE

Device	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	*Auto-Online* Circuitry	TTL 3-State	No. of Pins
SP3223U	+3.0V to +5.5V	2	2	4 capacitors	YES	YES	20
SP3243U	+3.0V to +5.5V	3	5	4 capacitors	YES	YES	28

Applicable U.S. Patents - 5,306,954; and other patents pending.

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ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}.....-0.3V to +6.0V
V+ (NOTE 1).....-0.3V to +7.0V
V- (NOTE 1).....+0.3V to -7.0V
V+ + |V-| (NOTE 1).....+13V
I_{CC} (DC V_{CC} or GND current).....±100mA

Input Voltages

TxIN, $\overline{\text{ONLINE}}$,
$\overline{\text{SHUTDOWN}}$, EN (**SP3223U**).....-0.3V to +6.0V
RxIN.....±25V

Output Voltages

TxOUT.....±13.2V
RxOUT, $\overline{\text{STATUS}}$.....-0.3V to (V_{CC} + 0.3V)

Short-Circuit Duration

TxOUT.....Continuous
Storage Temperature.....-65°C to +150°C

Power Dissipation per package

20-pin PDIP (derate 16.0mW/°C above+70°C).....1300mW
20-pin SSOP (derate 9.25mW/°C above +70°C)....750mW
20-pin TSSOP (derate 11.1mW/°C above +70°C)..900mW
28-pin SOIC (derate 12.7mW/°C above +70°C)....1000mW
28-pin SSOP (derate 11.2mW/°C above +70°C).....900mW
28-pin TSSOP (derate 13.2mW/°C above +70°C).....1059mW
32-pin QFN (derate 29.4mW/°C above +70°C).....2352mW

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.5V with T_{AMB} = T_{MIN} to T_{MAX}, C1 - C4 = 0.1µF. Typical values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current,AUTO ON-LINE®		1.0	10	µA	All RxIN open, $\overline{\text{ONLINE}}$ = GND, $\overline{\text{SHUTDOWN}}$ = V_{CC}, V_{CC} = +3.3V, T_{AMB} = +25°C, TxIN = GND or V_{CC}
Supply Current, Shutdown		1.0	10	µA	$\overline{\text{SHUTDOWN}}$ = GND, V_{CC} = +3.3V, T_{AMB} = +25°C, TxIN = V_{CC} or GND
Supply Current, AUTO ON-LINE® Disabled		0.3	1.0	mA	$\overline{\text{ONLINE}}$ = $\overline{\text{SHUTDOWN}}$ = V_{CC}, no load, V_{CC} = +3.3V, T_{AMB} = +25°C, TxIN = GND or V_{CC}
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW HIGH	 2.4		 0.8	 V V	V_{CC} = +3.3V or +5.0V, TxIN, $\overline{\text{EN}}$(SP3223U), $\overline{\text{ONLINE}}$, $\overline{\text{SHUTDOWN}}$
Input Leakage Current		±0.01	±1.0	µA	TxIN, $\overline{\text{EN}}$, $\overline{\text{ONLINE}}$, $\overline{\text{SHUTDOWN}}$, T_{AMB} = +25°C, V_{IN} = 0V to V_{CC}
Output Leakage Current		±0.05	±10	µA	Receivers disabled, V_{OUT} = 0V to V_{CC}
Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
Output Voltage HIGH	V_{CC} - 0.6	V_{CC} - 0.1		V	I_{OUT} = -1.0mA
DRIVER OUTPUTS					
Output Voltage Swing	±5.0	±5.4		V	All driver outputs loaded with 3KΩ to GND, T_{AMB} = +25°C
Output Resistance	300			Ω	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V
Output Short-Circuit Current		±35	±60	mA	V_{OUT} = 0V
Output Leakage Current			±25	µA	V_{CC} = 0V or 3.0V to 5.5V, V_{OUT} = ±12V, Drivers disabled

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ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.5V with $T_{AMB} = T_{MIN}$ to T_{MAX}, C1 - C4 = 0.1µF. Typical values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RECEIVER INPUTS					
Input Voltage Range	-25		25	V	
Input Threshold LOW	0.6	1.2		V	V_{CC} = 3.3V
Input Threshold LOW	0.8	1.5		V	V_{CC} = 5.0V
Input Threshold HIGH		1.5	2.4	V	V_{CC} = 3.3V
Input Threshold HIGH		1.8	2.4	V	V_{CC} = 5.0V
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	kΩ	
AUTO ON-LINE® CIRCUITRY CHARACTERISTICS ($\overline{ONLINE}$ = GND, $\overline{SHUTDOWN}$ = V_{CC})					
$\overline{STATUS}$ Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
$\overline{STATUS}$ Output Voltage HIGH	V_{CC} - 0.6			V	I_{OUT} = -1.0mA
Receiver Threshold to Drivers Enabled (t_{ONLINE})		200		µS	Figure 19
Receiver Positive or Negative Threshold to $\overline{STATUS}$ HIGH (t_{STSH})		0.5		µS	Figure 19
Receiver Positive or Negative Threshold to $\overline{STATUS}$ LOW (t_{STSL})		20		µS	Figure 19
TIMING CHARACTERISTICS					
Maximum Data Rate	1000			Kbps	R_L = 3KΩ, C_L = 250pF, one driver active
Receiver Propagation Delay t_{PHL} t_{PLH}		 0.15 0.15		µs	Receiver input to Receiver output, C_L = 150pF
Receiver Output Enable Time		200		ns	Normal operation
Receiver Output Disable Time		200		ns	Normal operation
Driver Skew		100		ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Receiver Skew		50		ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Transition-Region Slew Rate		90		V/µs	V_{CC} = 3.3V, R_L = 3KΩ, T_{AMB} = 25°C, measurements taken from -3.0V to +3.0V or +3.0V to -3.0V

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TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 1000kbps data rate, all drivers loaded with 3kΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

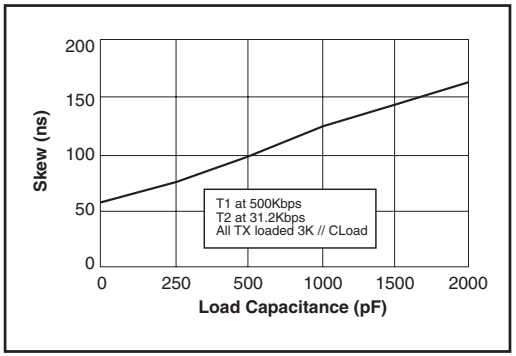

Figure 1. Transmitter Skew VS. Load Capacitance for the SP3223U / SP3243U

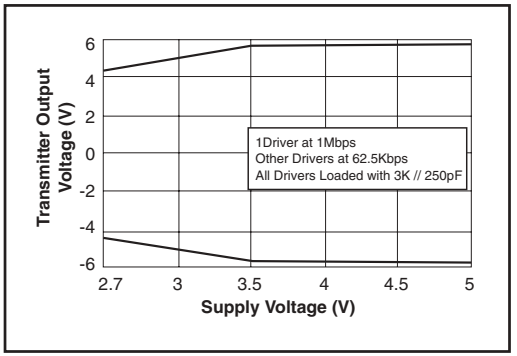

Figure 2. Transmitter Output Voltage VS. Supply Voltage for the SP3223U

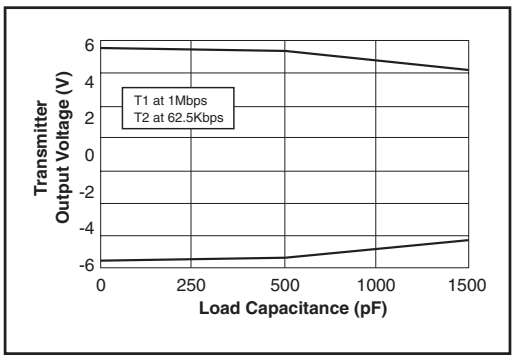

Figure 3. Transmitter Output Voltage VS. Load Capacitance for the SP3223U

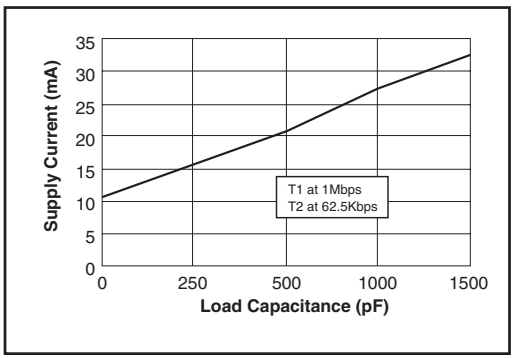

Figure 4. Supply Current VS. Load Capacitance for the SP3223U

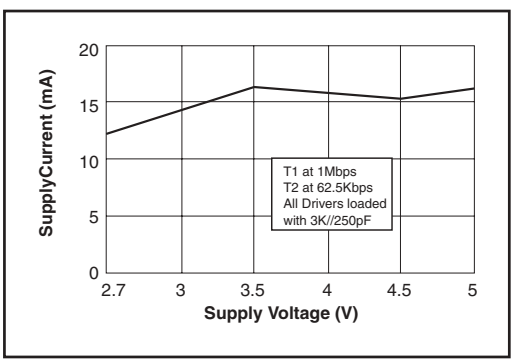

Figure 5. Supply Current VS. Supply Voltage for the SP3223U

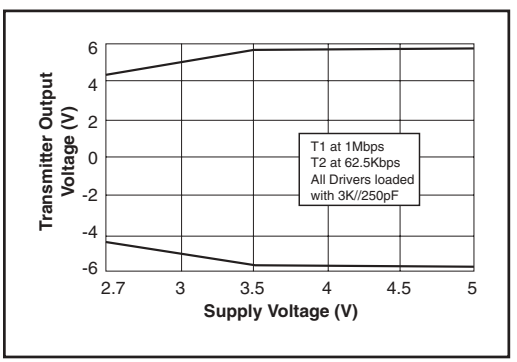

Figure 6. Transmitter Output Voltage VS. Supply Voltage for the SP3223U

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TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 1000kbps data rate, all drivers loaded with 3kΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

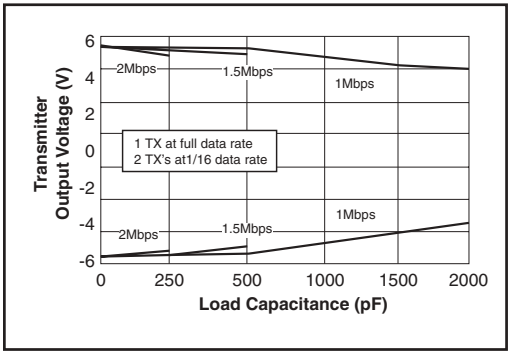

Figure 7. Transmitter Output Voltage VS. Load Capacitance for the SP3243U

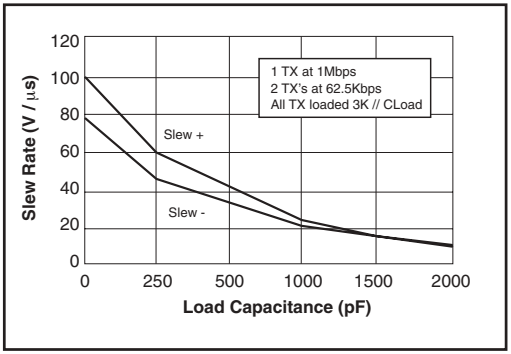

Figure 8. Slew Rate VS. Load Capacitance for the SP3243U

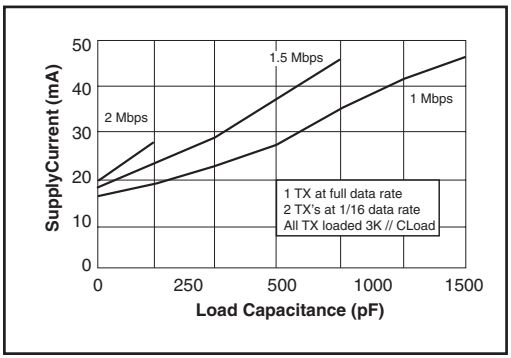

Figure 9. Supply Current VS. Load Capacitance for the SP3243U

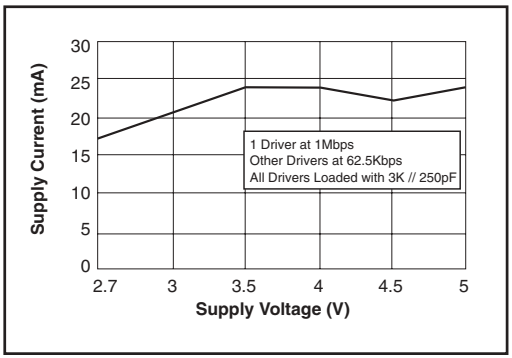

Figure 10. Supply Current VS. Supply Voltage for the SP3243U

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NAME	FUNCTION	PIN NUMBER		
		SP3223U	SP3243U	SP3243UCR QFN
$\overline{EN}$	Receiver Enable. Apply logic LOW for normal operation. Apply logic HIGH to disable the receiver outputs (high-Z state).	1	-	-
C1+	Positive terminal of the voltage doubler charge-pump capacitor.	2	28	28
V+	Regulated +5.5V output generated by the charge pump.	3	27	26
C1-	Negative terminal of the voltage doubler charge-pump capacitor.	4	24	22
C2+	Positive terminal of the inverting charge-pump capacitor.	5	1	29
C2-	Negative terminal of the inverting charge-pump capacitor.	6	2	31
V-	Regulated -5.5V output generated by the charge pump.	7	3	32
R_1IN	RS-232 receiver input.	16	4	2
R_2IN	RS-232 receiver input.	9	5	3
R_3IN	RS-232 receiver input.	-	6	4
R_4IN	RS-232 receiver input.	-	7	5
R_5IN	RS-232 receiver input.	-	8	6
R_1OUT	TTL/CMOS receiver output.	15	19	17
R_2OUT	TTL/CMOS receiver output.	10	18	16
$\overline{R_2OUT}$	Non-inverting receiver-2 output, active in shutdown.	-	20	18
R_3OUT	TTL/CMOS receiver output.	-	17	15
R_4OUT	TTL/CMOS receiver output.	-	16	14
R_5OUT	TTL/CMOS receiver output.	-	15	13
$\overline{STATUS}$	TTL/CMOS Output indicating online and shutdown status.	11	21	19
T_1IN	TTL/CMOS driver input.	13	14	12
T_2IN	TTL/CMOS driver input.	12	13	11
T_3IN	TTL/CMOS driver input.	-	12	10
$\overline{ONLINE}$	Apply logic HIGH to override Auto-Online circuitry keeping drivers active ($\overline{SHUTDOWN}$ must also be logic HIGH, refer to Table 2).	14	23	21
T_1OUT	RS-232 driver output.	17	9	7
T_2OUT	RS-232 driver output.	8	10	8
T_3OUT	RS-232 driver output.	-	11	9
GND	Ground.	18	25	23
V_{CC}	+3.0V to +5.5V supply voltage.	19	26	25
$\overline{SHUTDOWN}$	Apply logic LOW to shut down drivers and charge pump. This overrides all AUTO ON-LINE® circuitry and $\overline{ONLINE}$ (refer to Table 2).	20	22	20
NC	No Connection	-	-	1,24,27,30

Table 1. Device Pin Description

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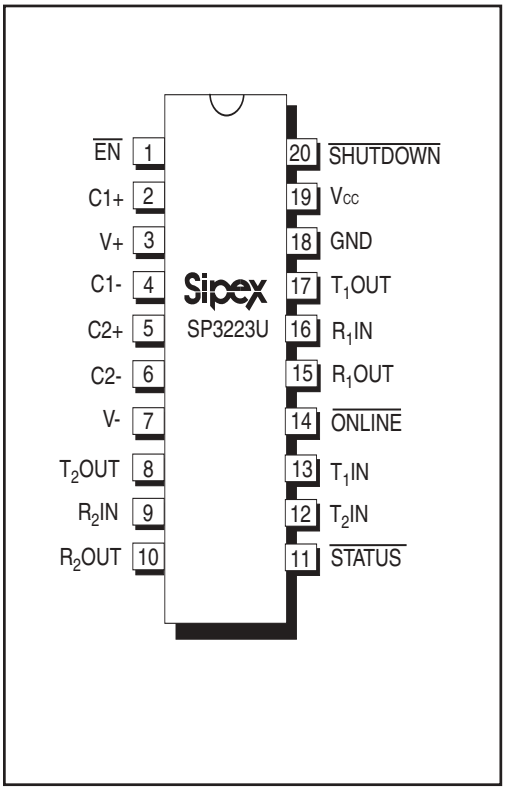

Figure 11. SP3223U Pinout Configuration

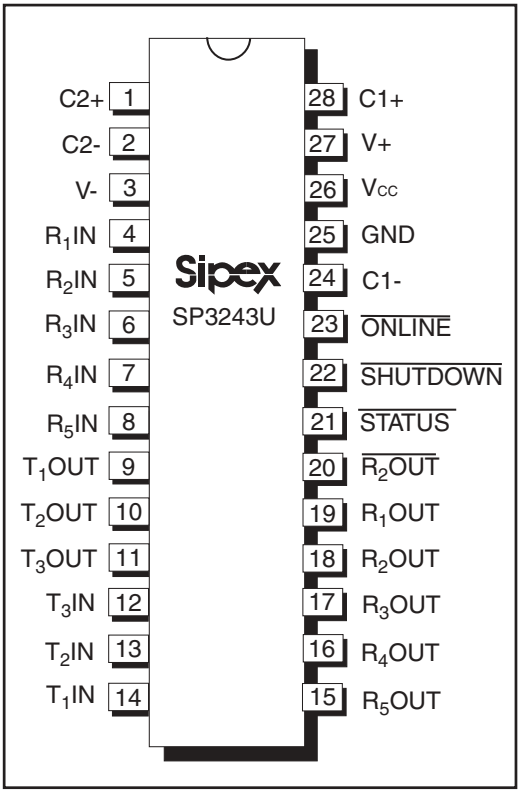

Figure 12. SP3243U Pinout Configuration

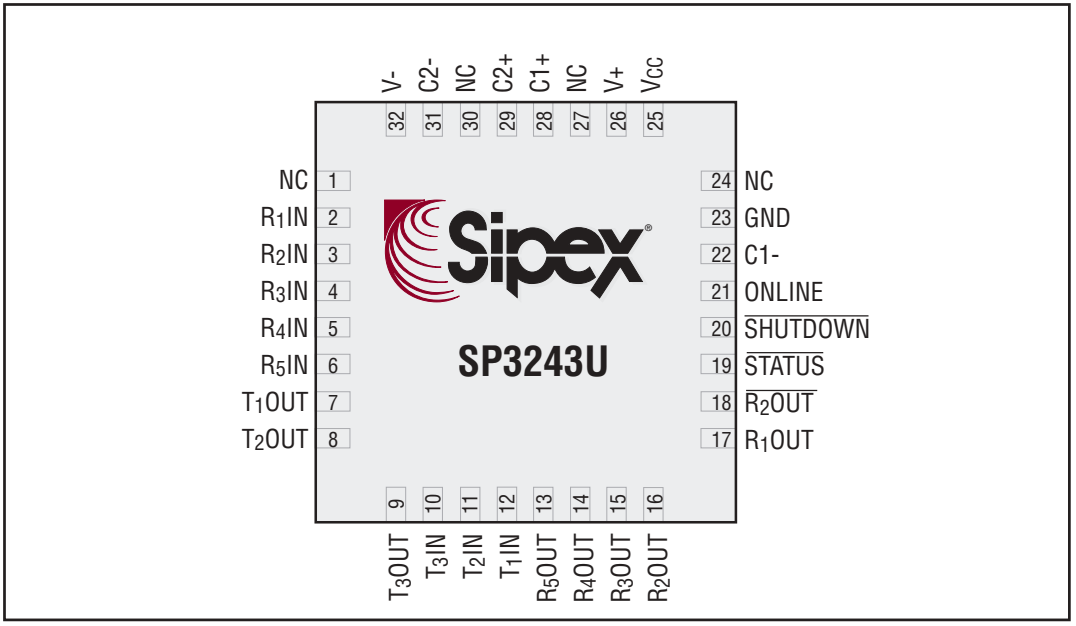

Figure 13. SP3243U QFN Pinout Configuration

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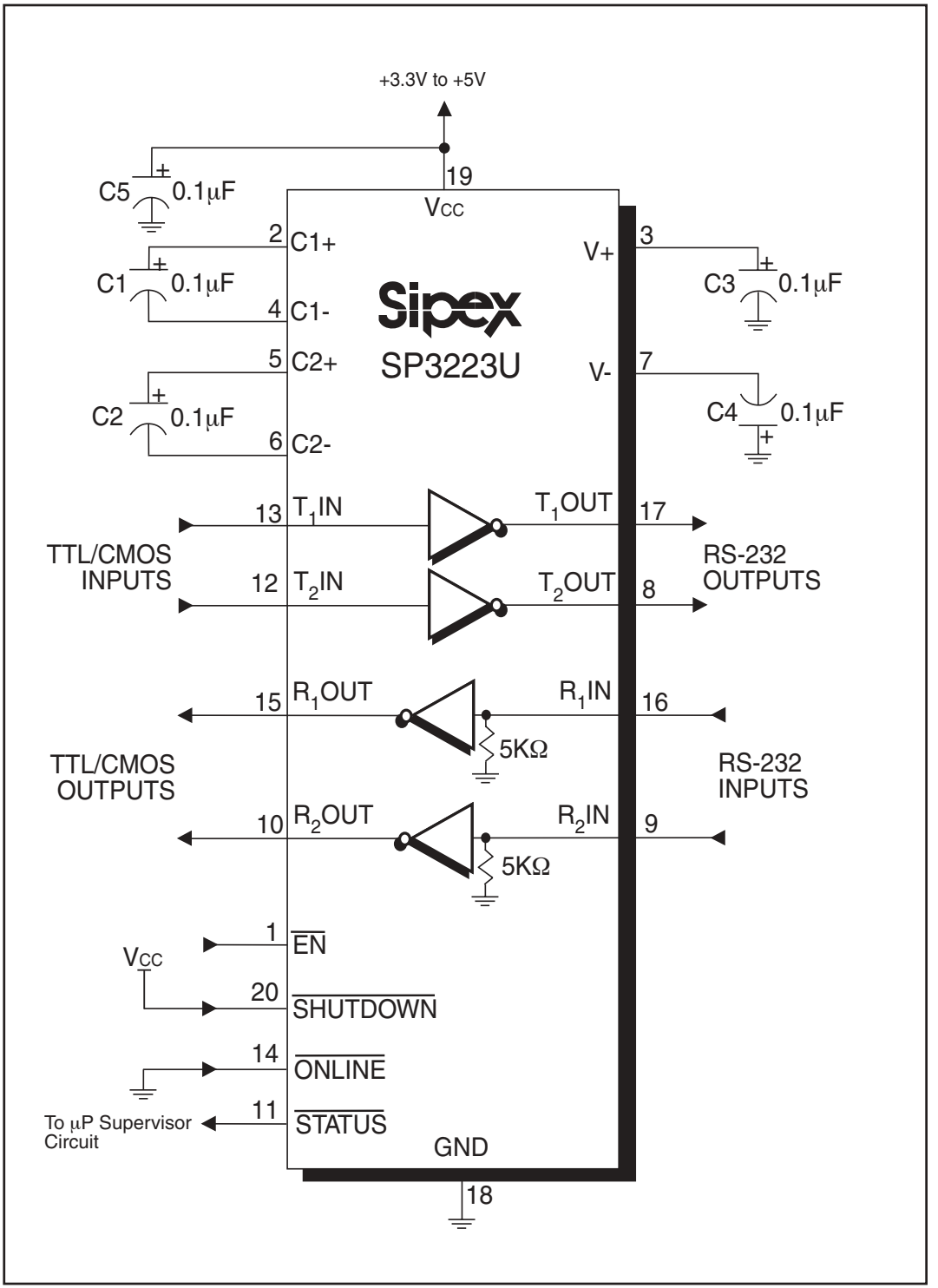

Figure 14. SP3223U Typical Operating Circuit

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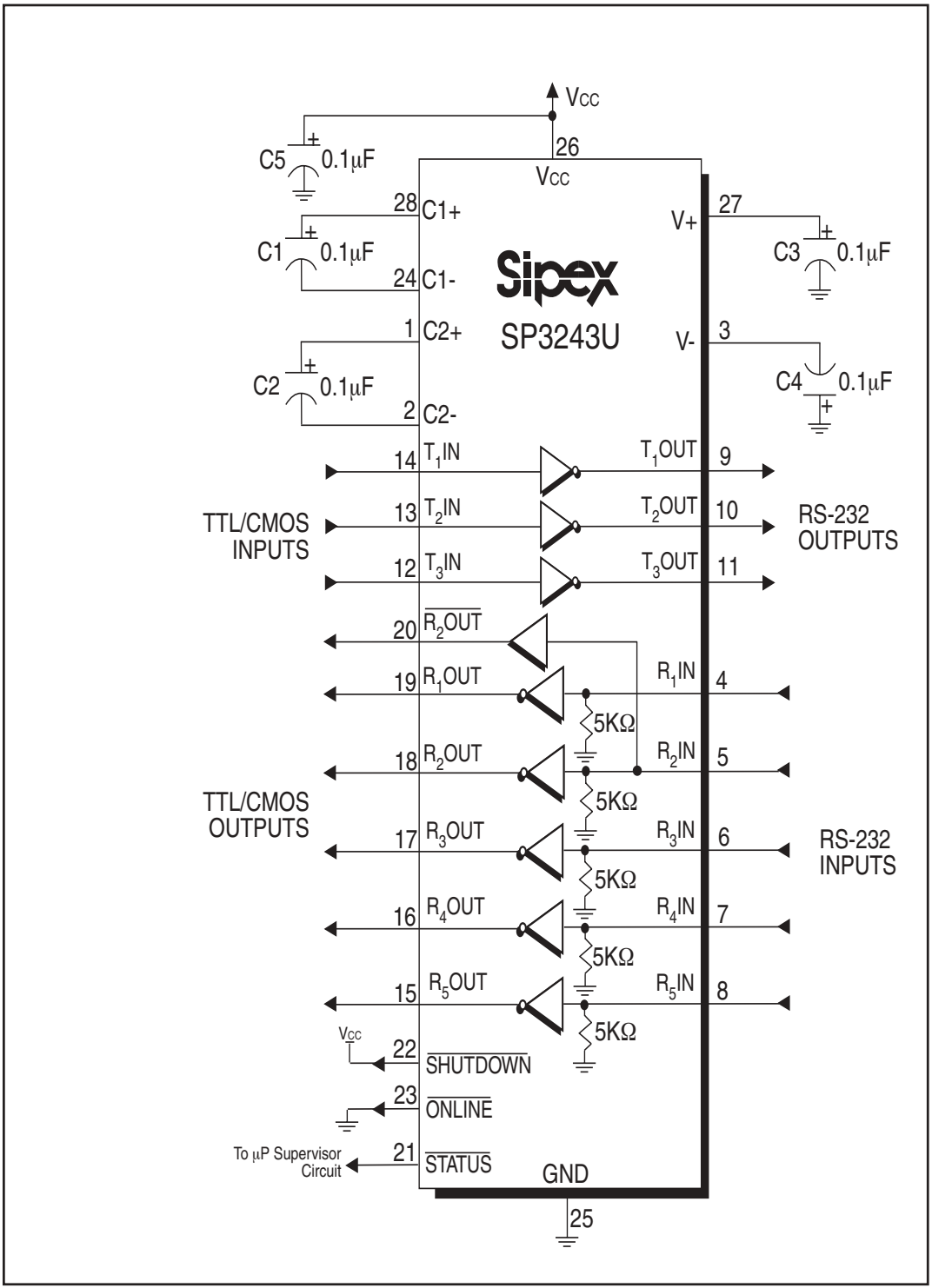

Figure 15. SP3243U Typical Operating Circuit

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DESCRIPTION

The SP3223U and SP3243U transceivers meet the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The SP3223U and SP3243U devices feature Sipex's proprietary and patented (U.S.-- 5,306,954) on-board charge pump circuitry that generates ±5.5V RS-232 voltage levels from a single +3.0V to +5.5V power supply. The SP3223U and SP3243U devices can operate at a data rate of 1000kbps fully loaded.

The SP3223U is a 2-driver/2-receiver device, and the SP3243U is a 3-driver/5-receiver device, ideal for portable or hand-held applications. The SP3243U includes one complementary always-active receiver that can monitor an external device (such as a modem) in shutdown. This aids in protecting the UART or serial controller IC by preventing forward biasing of the protection diodes where V_{CC} may be disconnected.

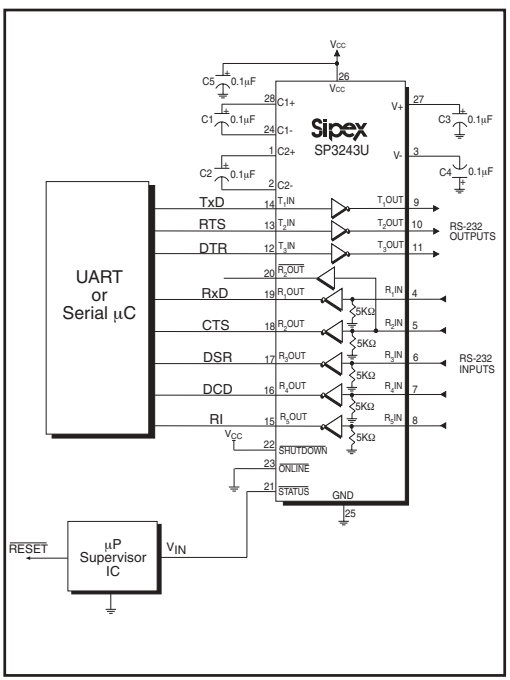

Figure 16. Interface Circuitry Controlled by Microprocessor Supervisory Circuit

The SP3223U and SP3243U series is an ideal choice for power sensitive designs. The SP3223U and SP3243U devices feature AUTO ON-LINE® circuitry which reduces the power supply drain to a 1µA supply current. In many portable or hand-held applications, an RS-232 cable can be disconnected or a connected peripheral can be turned off. Under these conditions, the internal charge pump and the drivers will be shut down. Otherwise, the system automatically comes online. This feature allows design engineers to address power saving concerns without major design changes.

THEORY OF OPERATION

The SP3223U and SP3243U series is made up of four basic circuit blocks:

1. Drivers
2. Receivers
3. the Sipex proprietary charge pump, and
4. AUTO ON-LINE® circuitry.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is ±5.4V with no load and ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232-F and all previous RS-232 versions. Unused drivers inputs should be connected to GND or V_{CC}.

The drivers have a minimum data rate of 1000kbps fully loaded with 3kΩ in parallel with 250pF, ensuring compatibility with PC-to-PC communication software.

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DEVICE: SP3223U			
$\overline{SHUTDOWN}$	$\overline{EN}$	T_XOUT	R_XOUT
0	0	High Z	Active
0	1	High Z	High Z
1	0	Active	Active
1	1	Active	High Z
DEVICE: SP3243U			
$\overline{SHUTDOWN}$	T_XOUT	R_XOUT	$\overline{R_2OUT}$
0	High Z	High Z	Active
1	Active	Active	Active

Table 2. $\overline{SHUTDOWN}$ and $\overline{EN}$ Truth Tables
Note: In AUTO ON-LINE® Mode where $\overline{ONLINE}$ = GND and $\overline{SHUTDOWN}$ = V_{CC}, the device will shut down if there is no activity present at the Receiver inputs.

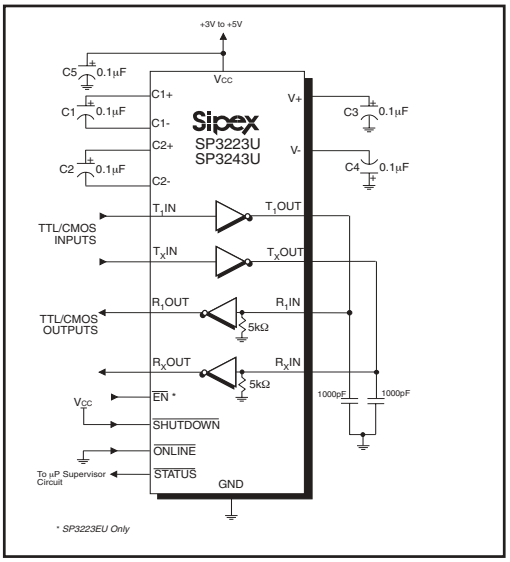

Figure 17. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

Figure 17 shows a loopback test circuit used to test the RS-232 Drivers. Figure 18 shows the test results where one driver was active at 1Mbps and all three drivers loaded with an RS-232 receiver in parallel with a 250pF capacitor. Figure 19 shows the test results of the loopback circuit with all drivers active at 250kbps with typical RS-232 loads in parallel with 1000pF capacitors. A superior RS-232 data transmission rate of 1Mbps makes the SP3223U/3243U series an ideal match for high speed LAN and personal computer peripheral applications.

Receivers

The receivers convert ±5.0V EIA/TIA-232 levels to TTL or CMOS logic output levels. The SP3223U receivers have an inverting output that can be disabled by using the EN pin.

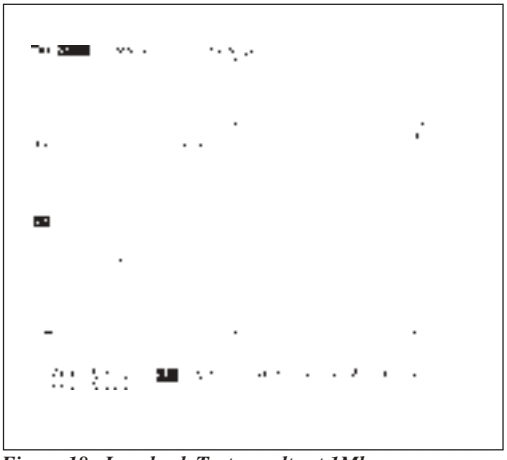

Figure 18. Loopback Test results at 1Mbps

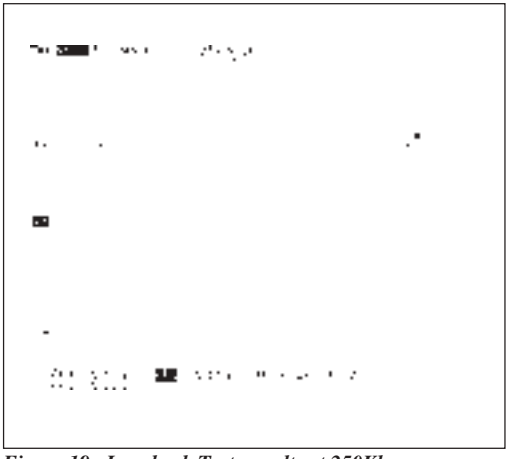

Figure 19. Loopback Test results at 250Kbps

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Receivers are active when the AUTO ON-LINE® circuitry is enabled or when in shutdown. During the shutdown, the receivers will continue to be active. If there is no activity present at the receivers for a period longer than 100µs or when SHUTDOWN is enabled, the device goes into a standby mode where the circuit draws 1µA. Driving EN to a logic HIGH forces the outputs of the receivers into high-impedance. The truth table logic of the SP3223U and SP3243U driver and receiver outputs can be found in Table 2.

The SP3243U includes an additional non-inverting receiver with an output R_2OUT. R_2OUT is an extra output that remains active and monitors activity while the other receiver outputs are forced into high impedance. This allows Ring Indicator (RI) from a peripheral to be monitored without forward biasing the TTL/CMOS inputs of the other devices connected to the receiver outputs.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5KΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

Charge Pump

The charge pump is a Sipex–patented design (U.S. 5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC}. C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now 2 times V_{CC}.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $–V_{CC}$ in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at V_{CC}, the voltage potential across C_2 is 2 times V_{CC}.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated

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from V_{CC}, in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 250kHz. The external capacitors can be as low as 0.1μF with a 16V breakdown voltage rating.

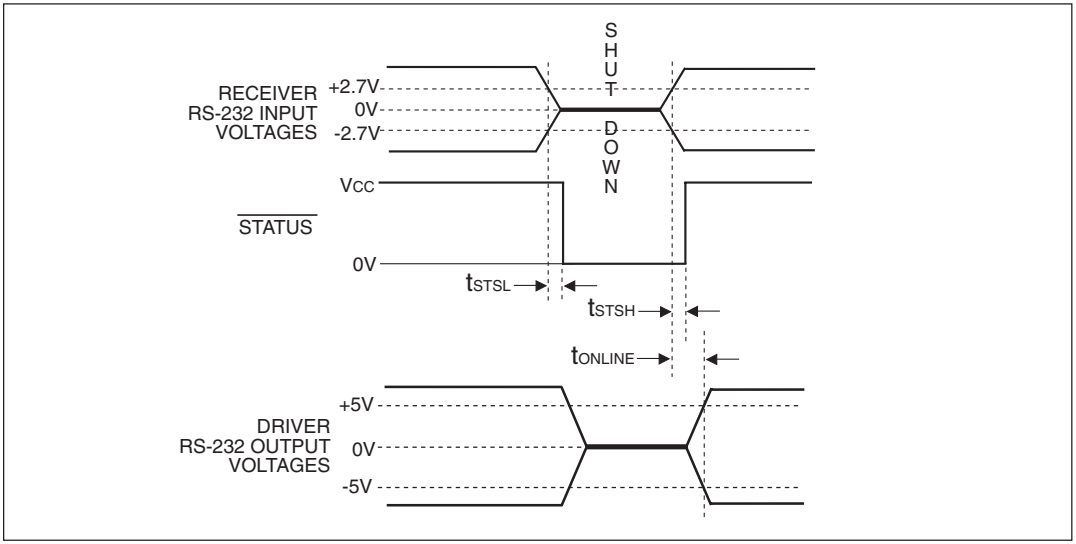

Figure 20. AUTO ON-LINE® Timing Waveforms

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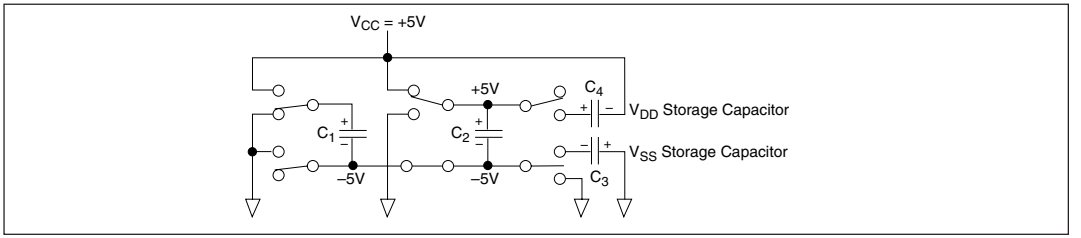

Figure 21. Charge Pump — Phase 1

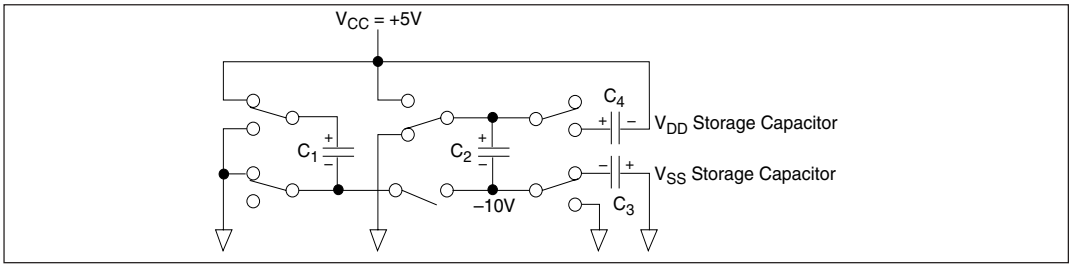

Figure 22. Charge Pump — Phase 2

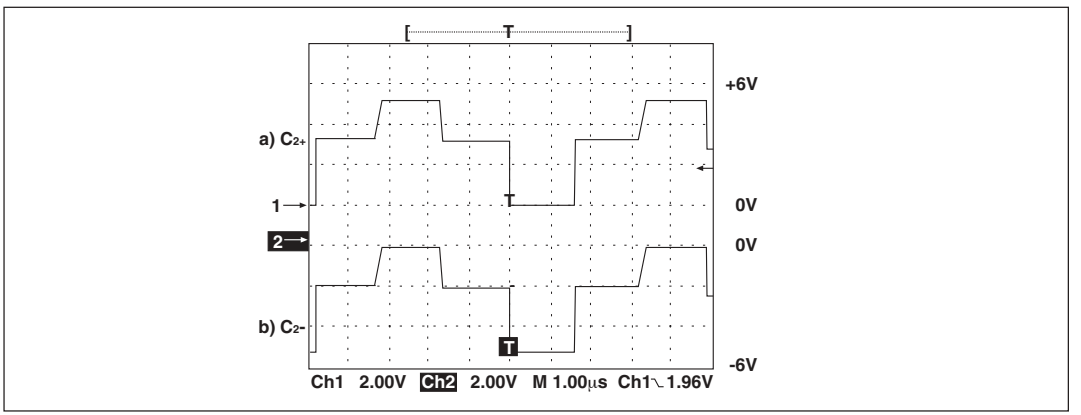

Figure 23. Charge Pump Waveforms

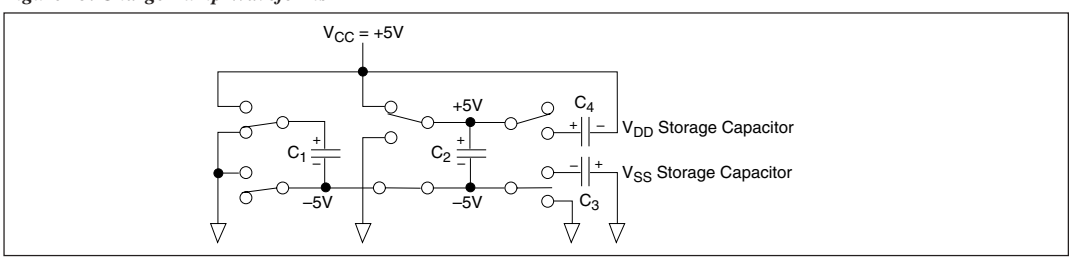

Figure 24. Charge Pump — Phase 3

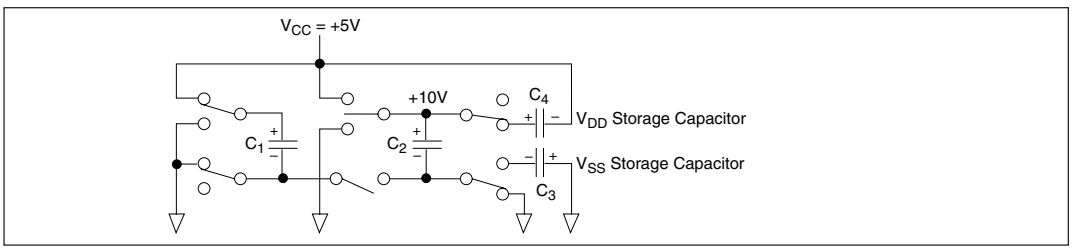

Figure 25. Charge Pump — Phase 4

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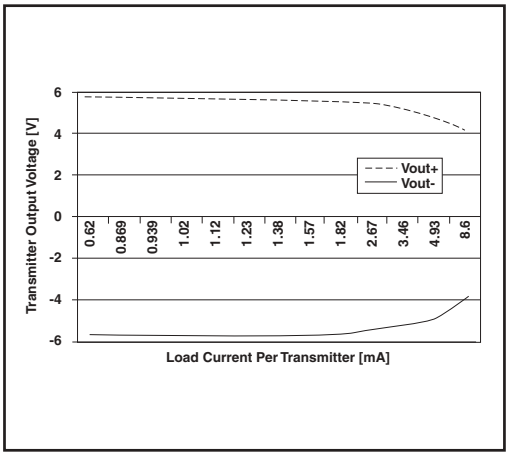

Figure 26. SP3243U Driver Output Voltages vs. Load Current per Transmitter

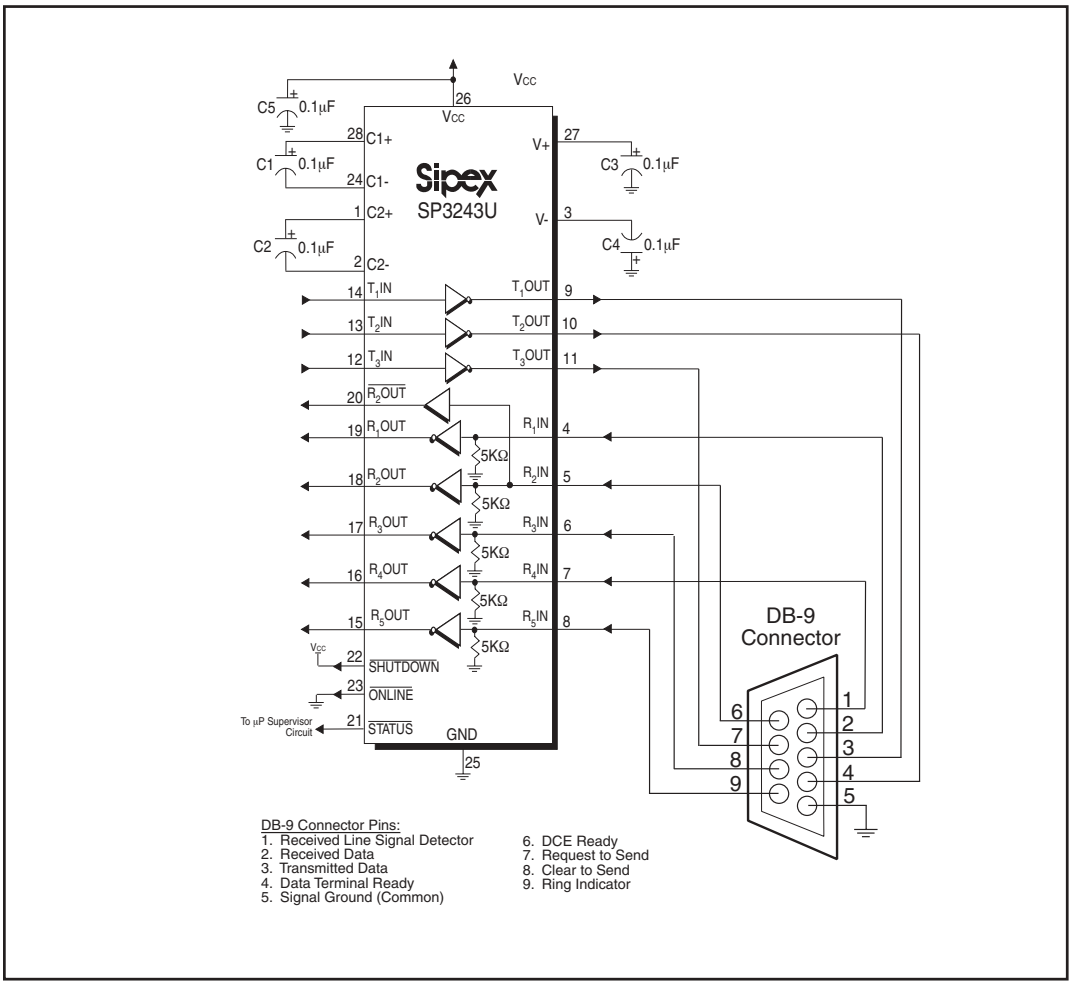

Figure 27. Circuit for the connectivity of the SP3243U with a DB-9 connector

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RS-232 SIGNAL AT RECEIVER INPUT	$\overline{\text{SHUTDOWN}}$ INPUT	$\overline{\text{ONLINE}}$ INPUT	$\overline{\text{STATUS}}$ OUTPUT	TRANSCEIVER STATUS
YES	HIGH	LOW	HIGH	Normal Operation ***(Auto-Online)***
NO	HIGH	HIGH	LOW	Normal Operation
NO	HIGH	LOW	LOW	Shutdown (***Auto-Online***)
YES	LOW	HIGH / LOW	HIGH	Shutdown
NO	LOW	HIGH / LOW	LOW	Shutdown

Table 3. AUTO ON-LINE® Logic

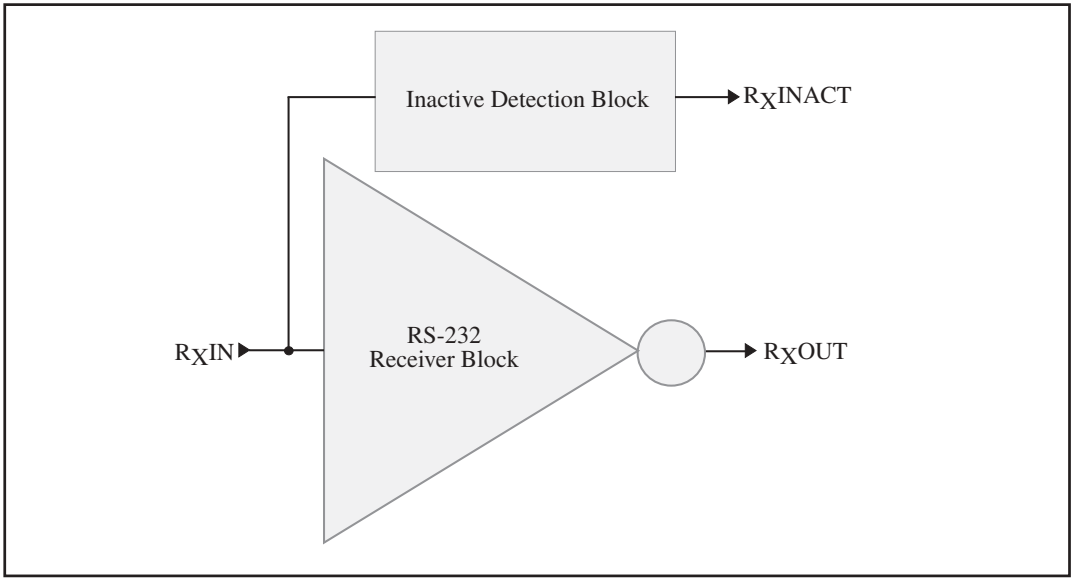

Figure 28. Stage I of AUTO ON-LINE® Circuitry

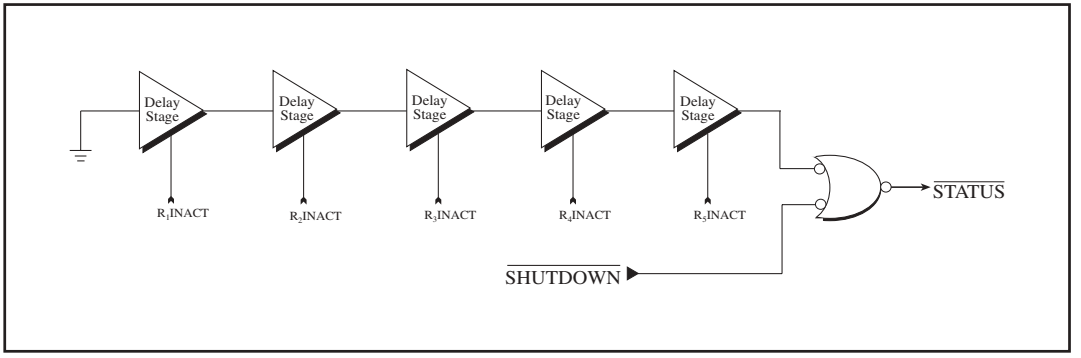

Figure 29. Stage II of AUTO ON-LINE® Circuitry

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AUTO ON-LINE® Circuitry

The SP3223U and SP3243U devices have a patent pending AUTO ON-LINE® circuitry on board that saves power in applications such as laptop computers, palmtop (PDA) computers and other portable systems.

The SP3223U and SP3243U devices incorporate an AUTO ON-LINE® circuit that automatically enables itself when the external transmitters are enabled and the cable is connected. Conversely, the AUTO ON-LINE® circuit also disables most of the internal circuitry when the device is not being used and goes into a standby mode where the device typically draws 1mA. This function can also be externally controlled by the $\overline{\text{ONLINE}}$ pin. When this pin is tied to a logic LOW, the AUTO ON-LINE® function is active. Once active, the device is enabled until there is no activity on the receiver inputs. The receiver input typically sees at least ±3V, which are generated from the transmitters at the other end of the cable with a ±5V minimum. When the external transmitters are disabled or the cable is disconnected, the receiver inputs will be pulled down by their internal 5kΩ resistors to ground. When this occurs over a period of time, the internal transmitters will be disabled and the device goes into a shutdown or standy mode. When $\overline{\text{ONLINE}}$ is HIGH, the AUTO ON-LINE® mode is disabled.

The AUTO ON-LINE® circuit has two stages:

1) Inactive Detection
2) Accumulated Delay

The first stage, shown in Figure 28, detects an inactive input. A logic HIGH is asserted on R_XINACT if the cable is disconnected or the external transmitters are disabled. Otherwise, R_XINACT will be at a logic LOW. This circuit is duplicated for each of the other receivers.

The second stage of the AUTO ON-LINE® circuitry, shown in Figure 29, processes all the receiver's R_XINACT signals with an accumulated delay that disables the device to a 1µA supply current.

The $\overline{\text{STATUS}}$ pin goes to a logic LOW when the cable is disconnected, the external transmitters are disabled, or the $\overline{\text{SHUTDOWN}}$ pin is invoked. The typical accumulated delay is around 20µs.

When the SP3223U and SP3243U drivers or internal charge pump are disabled, the supply current is reduced to 1µA. This can commonly occur in hand-held or portable applications where the RS-232 cable is disconnected or the RS-232 drivers of the connected peripheral are turned off.

The AUTO ON-LINE® mode can be disabled by the $\overline{\text{SHUTDOWN}}$ pin. If this pin is a logic LOW, the AUTO ON-LINE® function will not operate regardless of the logic state of the $\overline{\text{ONLINE}}$ pin. Table 3 summarizes the logic of the AUTO ON-LINE® operating modes. The truth table logic of the SP3223U and SP3243U driver and receiver outputs can be found in Table 2.

The $\overline{\text{STATUS}}$ pin outputs a logic LOW signal if the device is shutdown. This pin goes to a logic HIGH when the external transmitters are enabled and the cable is connected.

When the SP3223U and SP3243U devices are shut down, the charge pumps are turned off. V+ charge pump output decays to V_{CC}, the V- output decays to GND. The decay time will depend on the size of capacitors used for the charge pump. Once in shutdown, the time required to exit the shut down state and have valid V+ and V- levels is typically 200µs.

For easy programming, the $\overline{\text{STATUS}}$ can be used to indicate DTR or a Ring Indicator signal. Tying $\overline{\text{ONLINE}}$ and $\overline{\text{SHUTDOWN}}$ together will bypass the AUTO ON-LINE® circuitry so this connection acts like a shutdown input pin.

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ESD TOLERANCE

The SP3223U/3243U series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients.

The Human Body Model has been the generally accepted ESD testing method for semi-conductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 30. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ and 100pF, respectively.

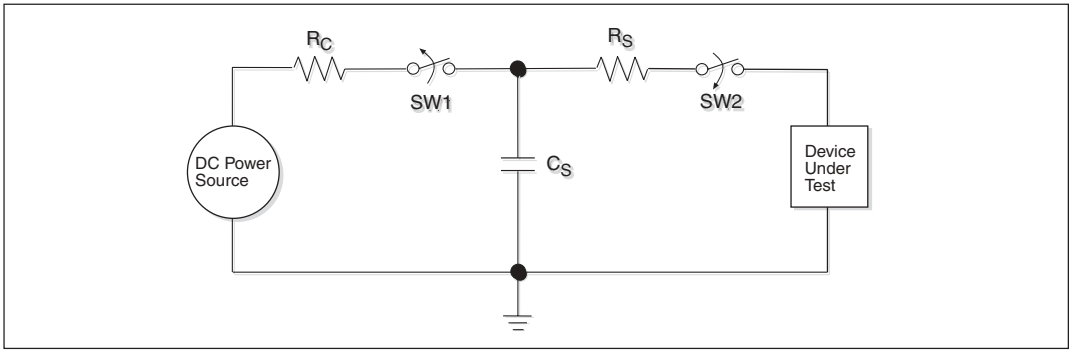

Figure 30. ESD Test Circuit for Human Body Model

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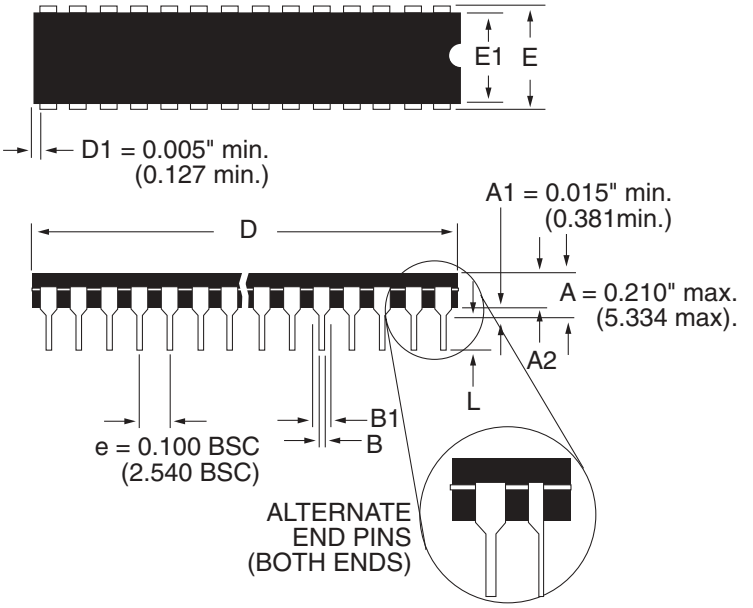
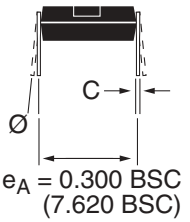
PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)





DIMENSIONS (Inches) Minimum/Maximum (mm)	16–PIN	20–PIN	28–PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.780/0.800 (19.812/20.320)	0.980/1.060 (24.892/26.924)	1.385/1.454 (35.17/36.90)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

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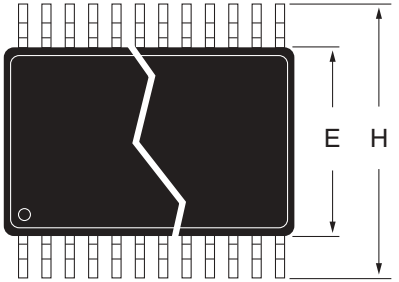
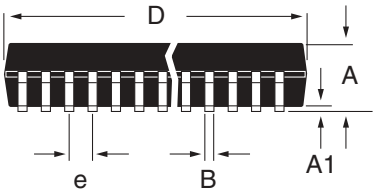
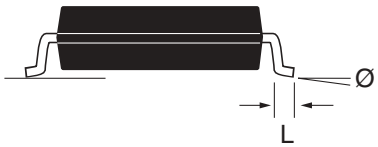
PACKAGE: PLASTIC SHRINK SMALL OUTLINE (SSOP)







DIMENSIONS (Inches) Minimum/Maximum (mm)	16–PIN	20–PIN	24–PIN	28–PIN
A	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)
A1	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)
B	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)
D	0.239/0.249 (6.07/6.33)	0.278/0.289 (7.07/7.33)	0.317/0.328 (8.07/8.33)	0.397/0.407 (10.07/10.33)
E	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)
e	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)
H	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)
L	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

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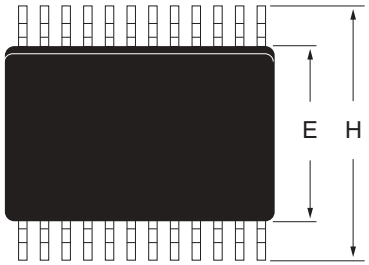
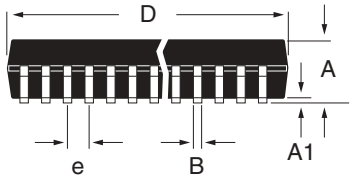
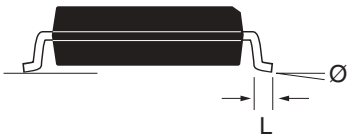
PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (WIDE)







DIMENSIONS (Inches) Minimum/Maximum (mm)	28–PIN
A	0.090/0.104 (2.29/2.649)
A1	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)
D	0.697/0.713 (17.70/18.09)
E	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

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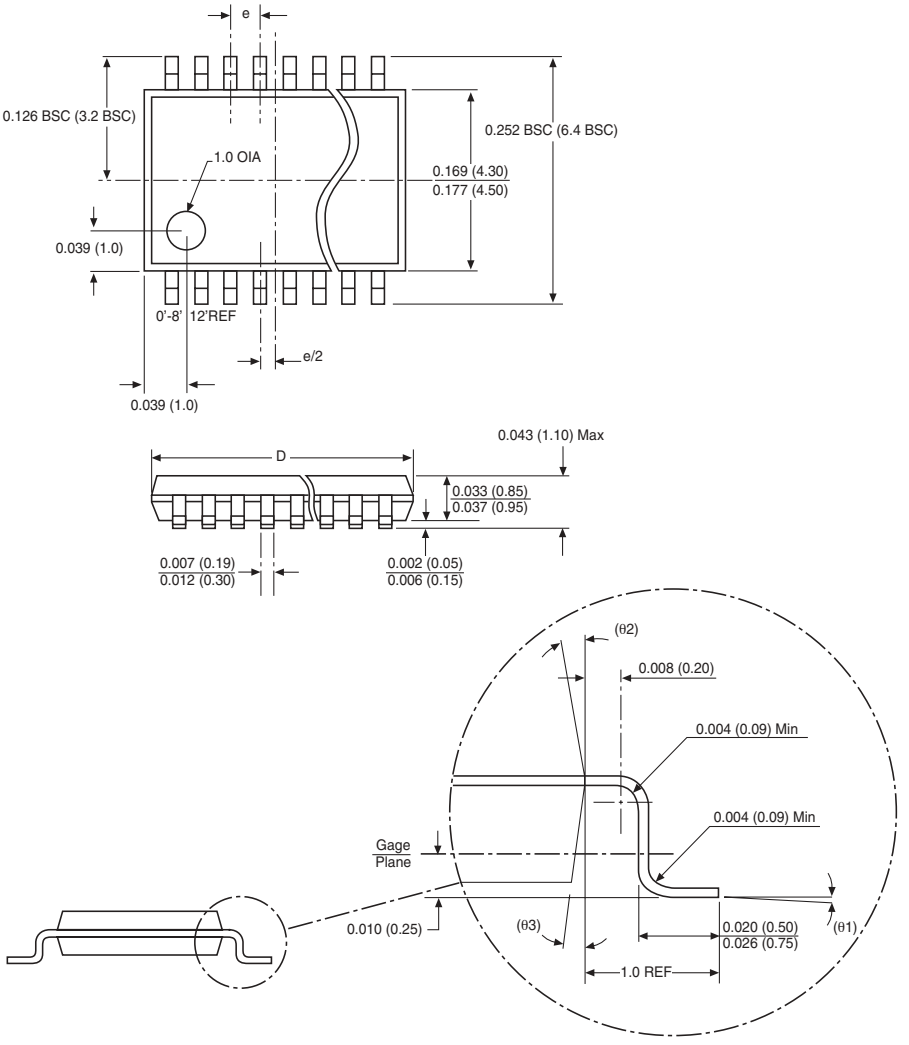
PACKAGE: PLASTIC THIN SMALL OUTLINE (TSSOP)

DIMENSIONS in inches (mm) Minimum/Maximum		
Symbol	**20 Lead**	**28 Lead**
D	0.252/0.260 (6.40/6.60)	0.378/0.386 (9.60/9.80)
e	0.026 BSC (0.65 BSC)	0.026 BSC (0.65 BSC)



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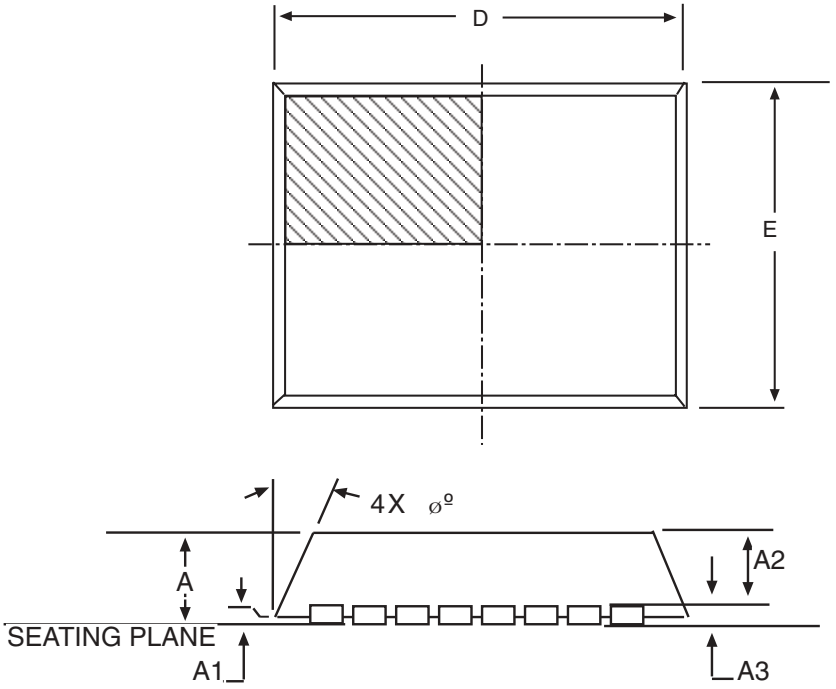

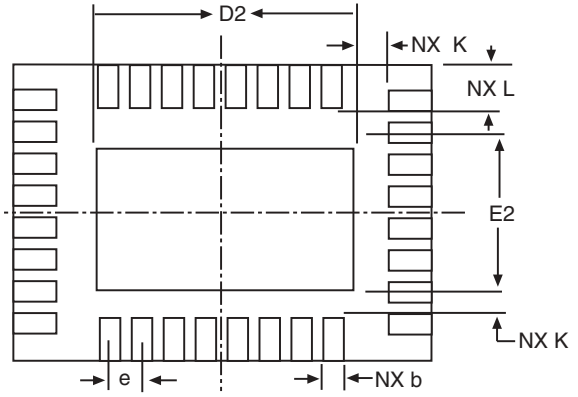

32 PIN QFN JEDECMO220 (VHHD-4)	Dimensions in (mm)		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0	0.65	1.00
A3		0.20 REF	
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
b	0.18	0.25	0.30
Ø	0°	-	14°
D2	3.50	3.65	3.80
E2	3.50	3.65	3.80
L	0.35	0.40	0.45
K	0.20	-	-
N		32	
ND		8	
NE		8	

32 PIN QFN

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ORDERING INFORMATION

Part Number	Temperature Range	Package Types
SP3223UCP	0°C to +70°C	20-pin PDIP
SP3223UCA	0°C to +70°C	20-pin SSOP
SP3223UCA/TR	0°C to +70°C	20-pin SSOP
SP3223UCY	0°C to +70°C	20-pin TSSOP
SP3223UCY/TR	0°C to +70°C	20-pin TSSOP
SP3243UCT	0°C to +70°C	28-pin WSOIC
SP3243UCT/TR	0°C to +70°C	28-pin WSOIC
SP3243UCA	0°C to +70°C	28-pin SSOP
SP3243UCA/TR	0°C to +70°C	28-pin SSOP
SP3243UCY	0°C to +70°C	28-pin TSSOP
SP3243UCY/TR	0°C to +70°C	28-pin TSSOP
SP3243UCR	0°C to +70°C	32-pin QFN
SP3243UCR/TR	0°C to +70°C	32-pin QFN
SP3223UEP	-40°C to +85°C	20-pin PDIP
SP3223UEA	-40°C to +85°C	20-pin SSOP
SP3223UEA/TR	-40°C to +85°C	20-pin SSOP
SP3223UEY	-40°C to +85°C	20-pin TSSOP
SP3223UEY/TR	-40°C to +85°C	20-pin TSSOP
SP3243UET	-40°C to +85°C	28-pin WSOIC
SP3243UET/TR	-40°C to +85°C	28-pin WSOIC
SP3243UEA	-40°C to +85°C	28-pin SSOP
SP3243UEA/TR	-40°C to +85°C	28-pin SSOP
SP3243UEY	-40°C to +85°C	28-pin TSSOP
SP3243UEY/TR	-40°C to +85°C	28-pin TSSOP
SP3243UER	-40°C to +85°C	32-pin QFN
SP3243UER/TR	-40°C to +85°C	32-pin QFN

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP3243UER/TR = standard; SP3243UER-L/TR = lead free

/TR = Tape and Reel

Pack quantity is 1,500 for SSOP, TSSOP and WSOIC.

REVISION HISTORY

DATE	REVISION	DESCRIPTION
5/25/04	A	Replaced MLPQ package with QFN.

ANALOG EXCELLENCE

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FAX: (408) 935-7600

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